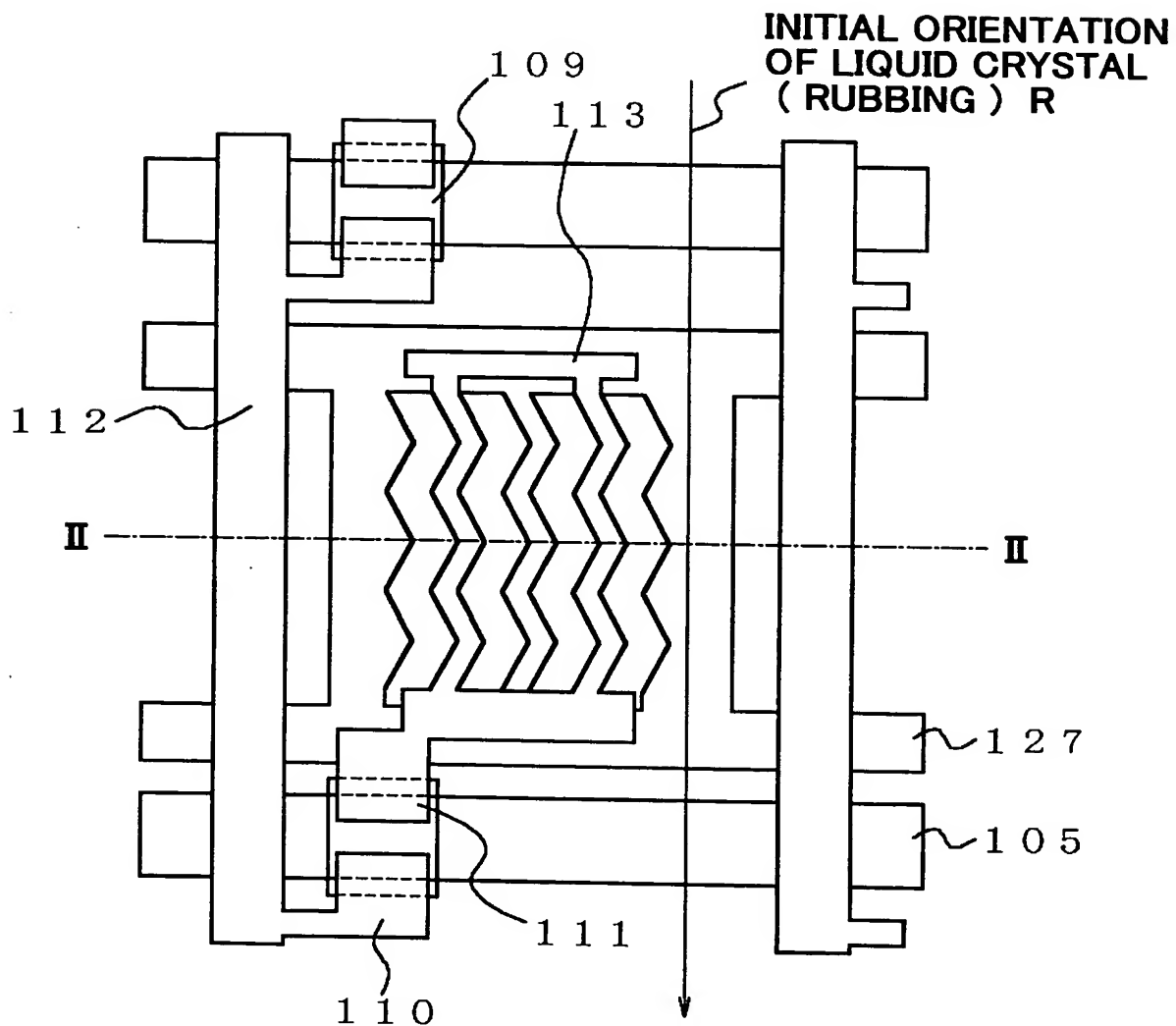


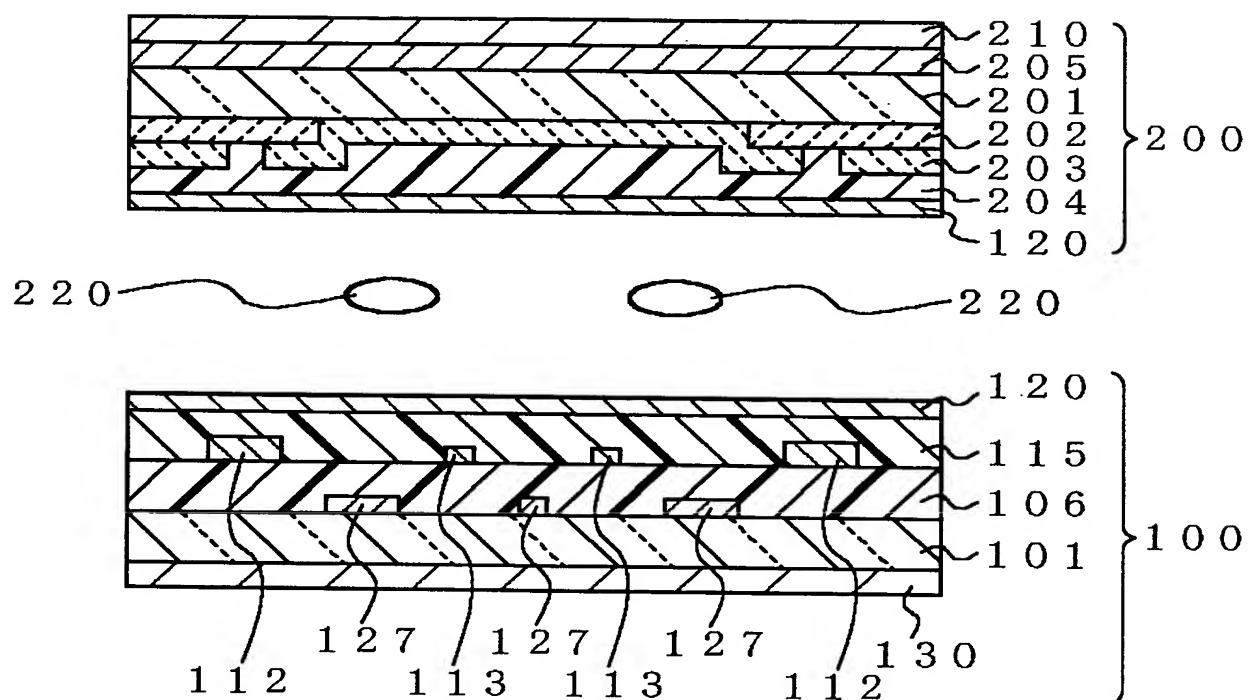
1/36

FIG. 1
PRIOR ART



2/36

FIG.2
 PRIOR ART



3/36

FIG.3

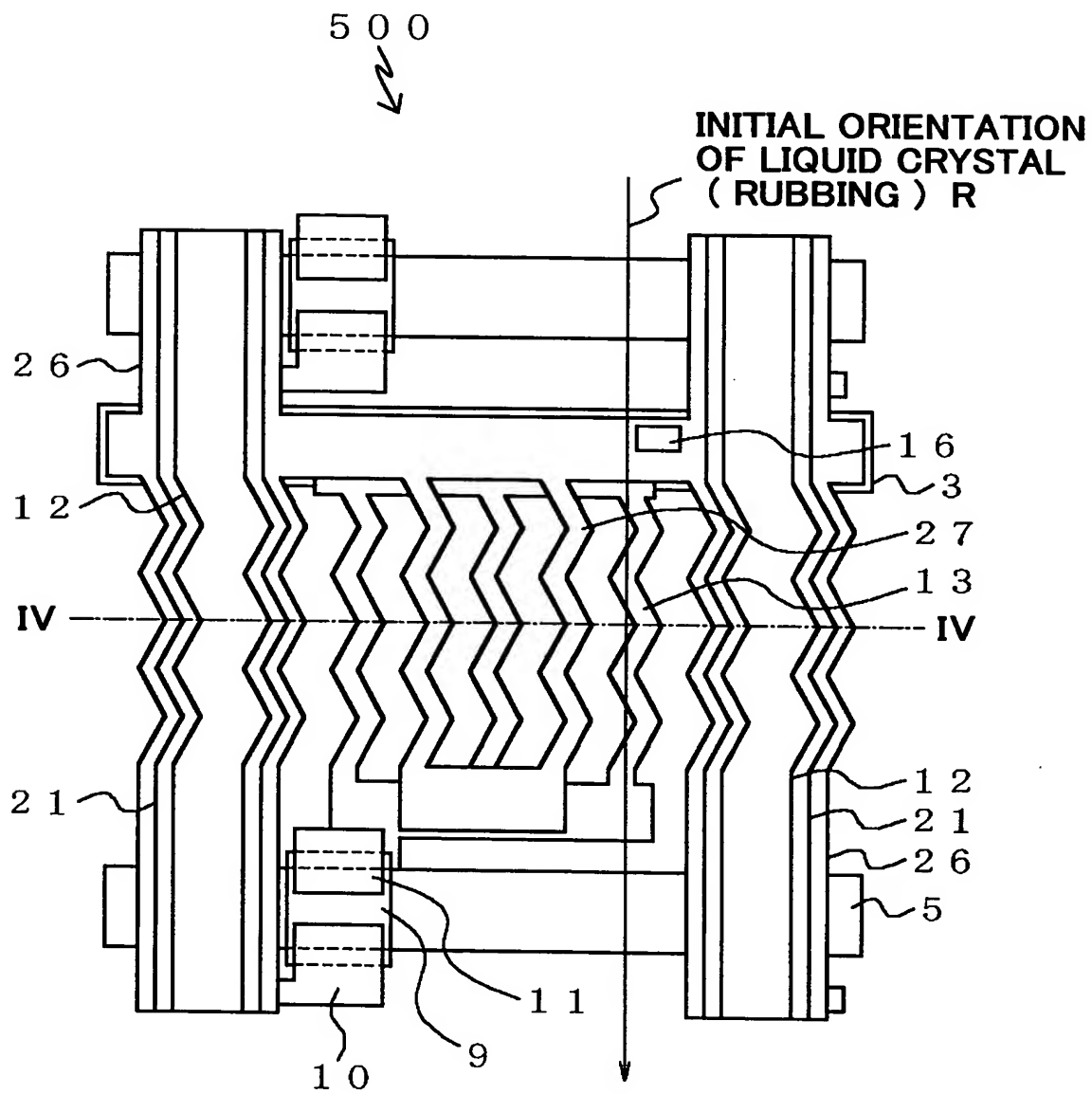
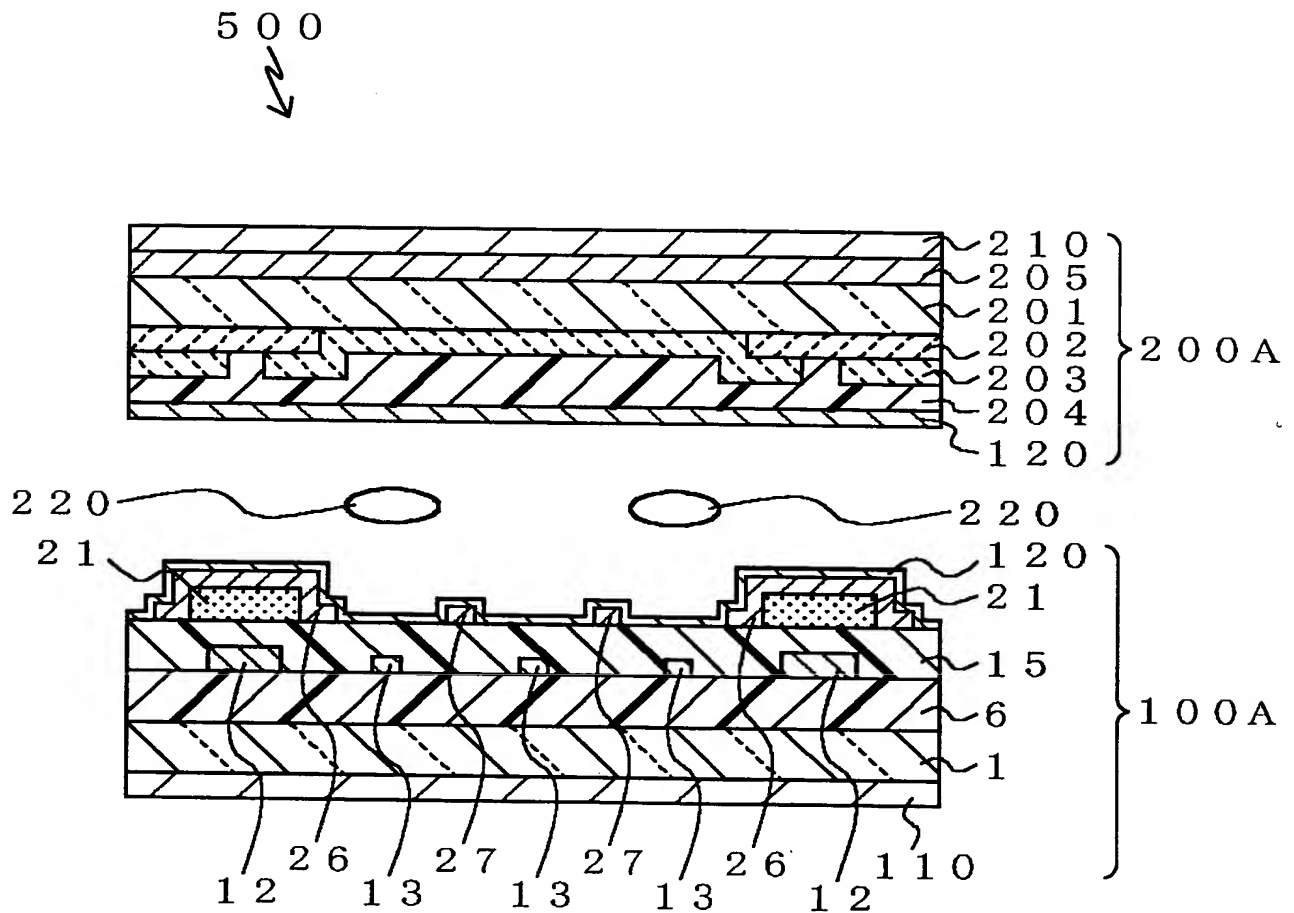


FIG.4



5/36

FIG.5A

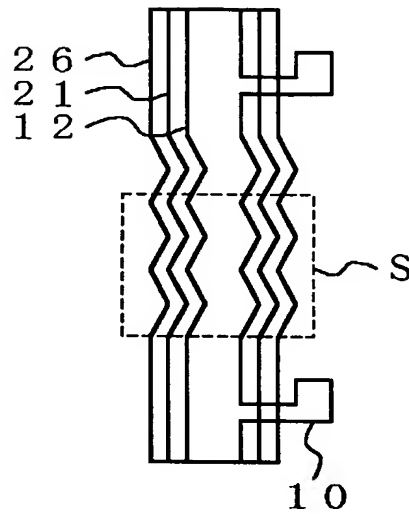


FIG.5B

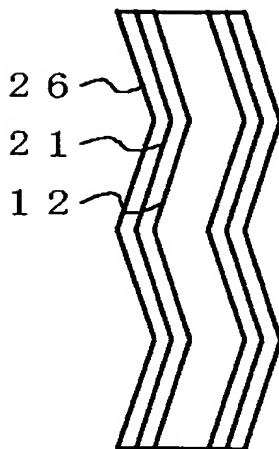
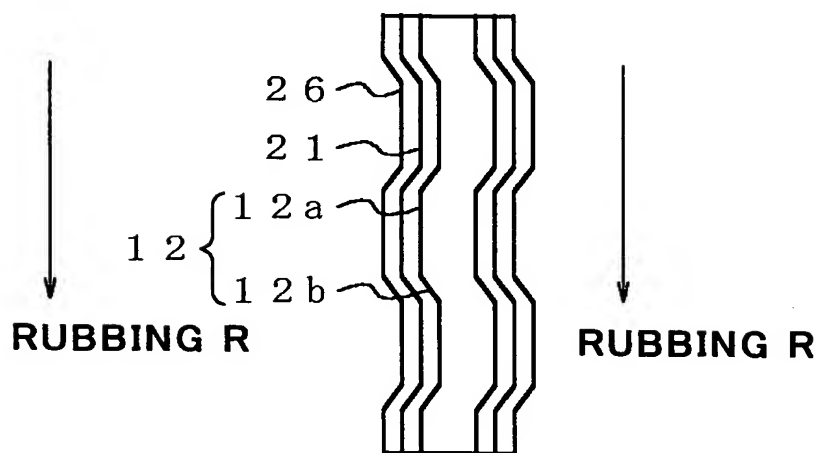
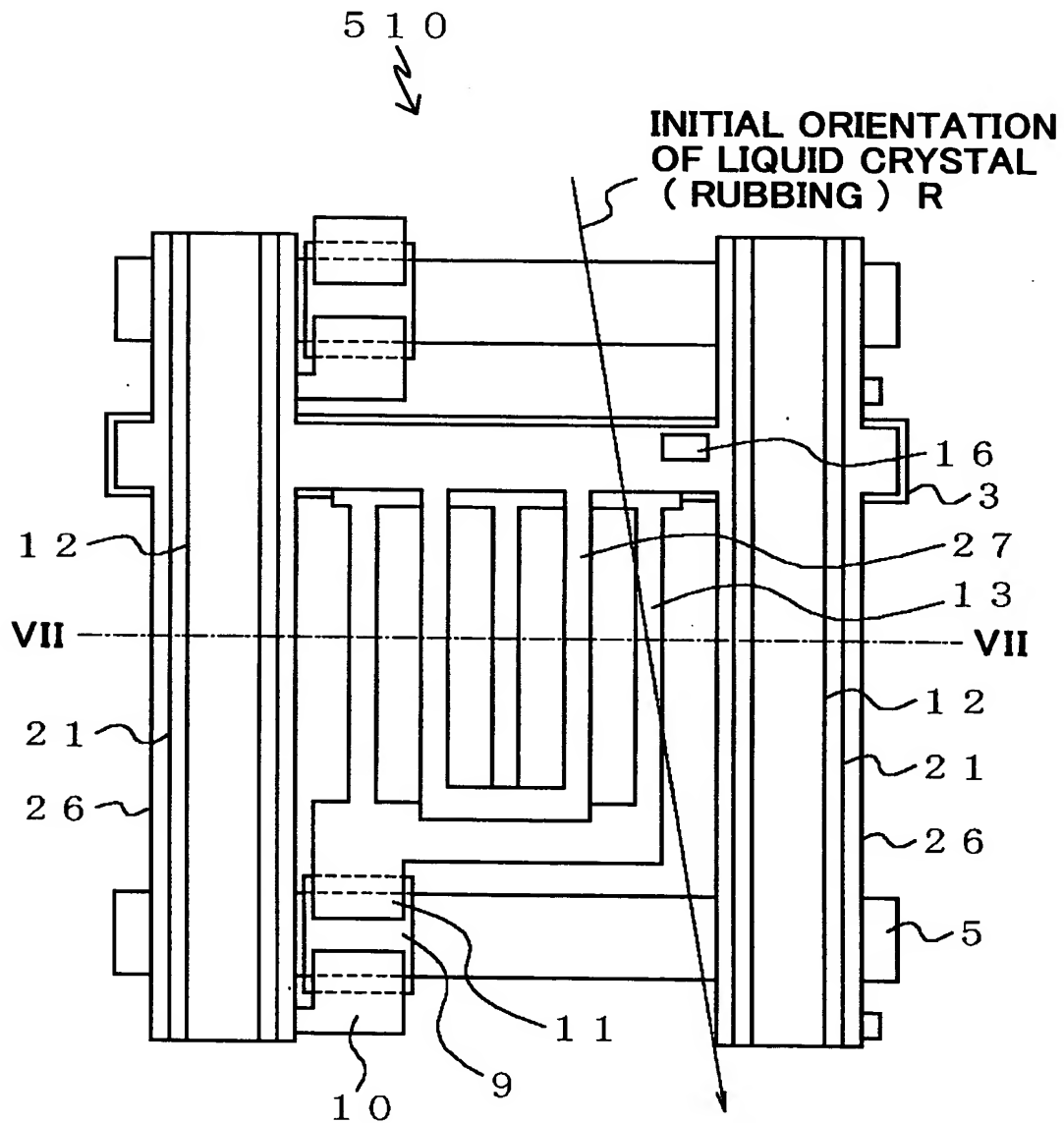


FIG.5C



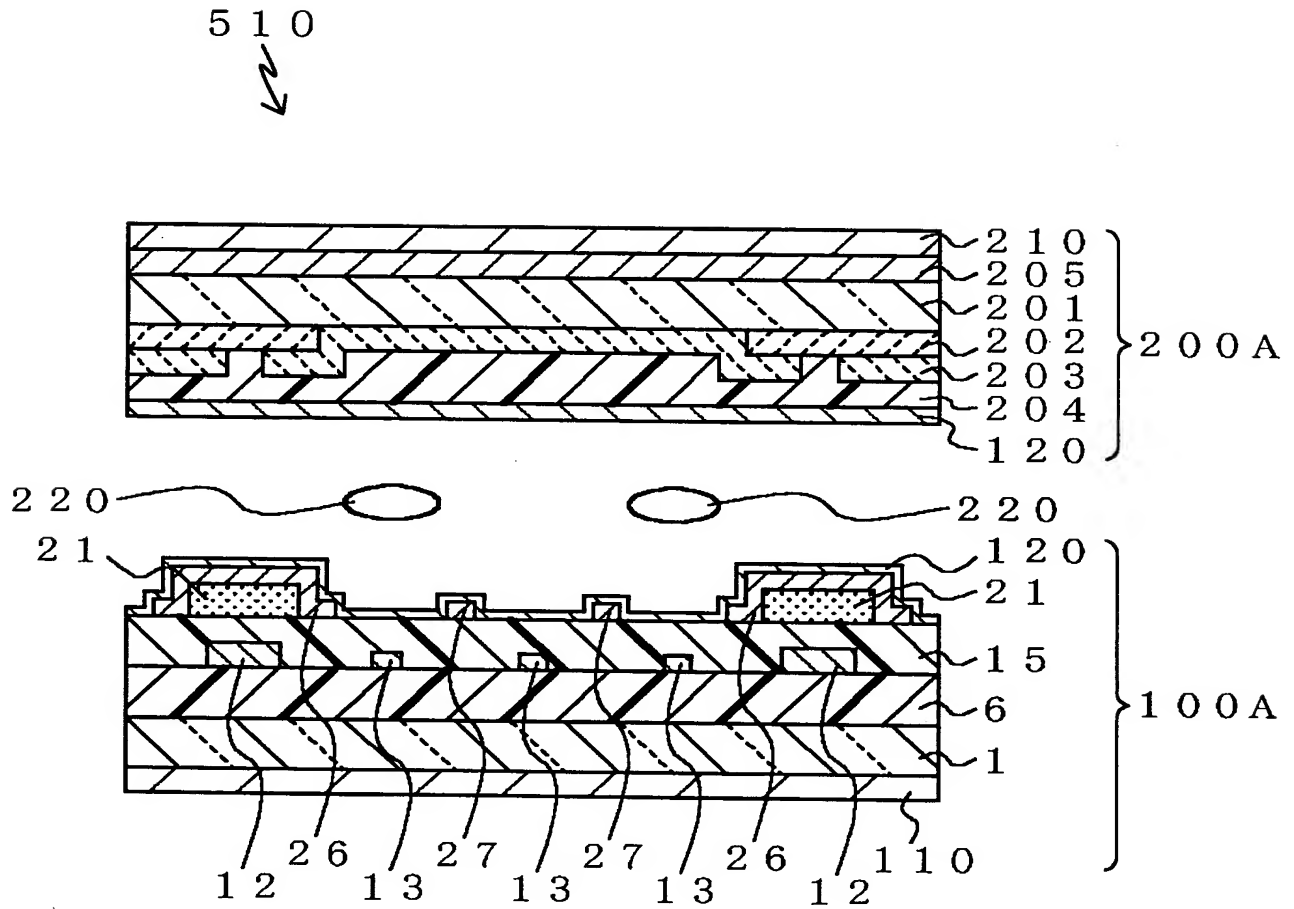
6/36

FIG.6



7/36

FIG.7



5 2 0

INITIAL ORIENTATION OF LIQUID CRYSTAL (RUBBING) R

IX

IX

1 2

2 1

2 6

1 7

1 1

9

1 0

1 6

3

2 7

3 1 3

1 2

2 1

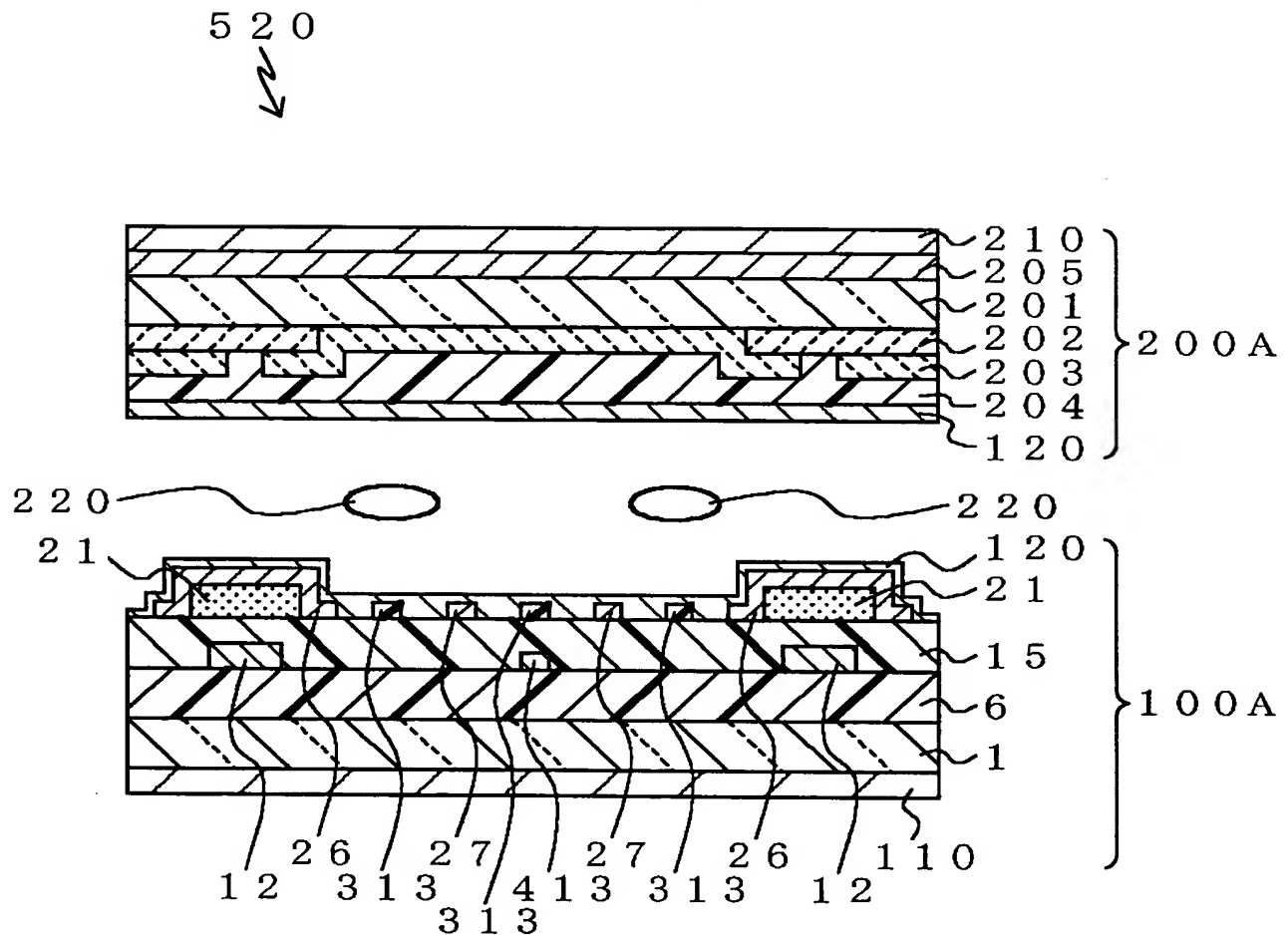
3

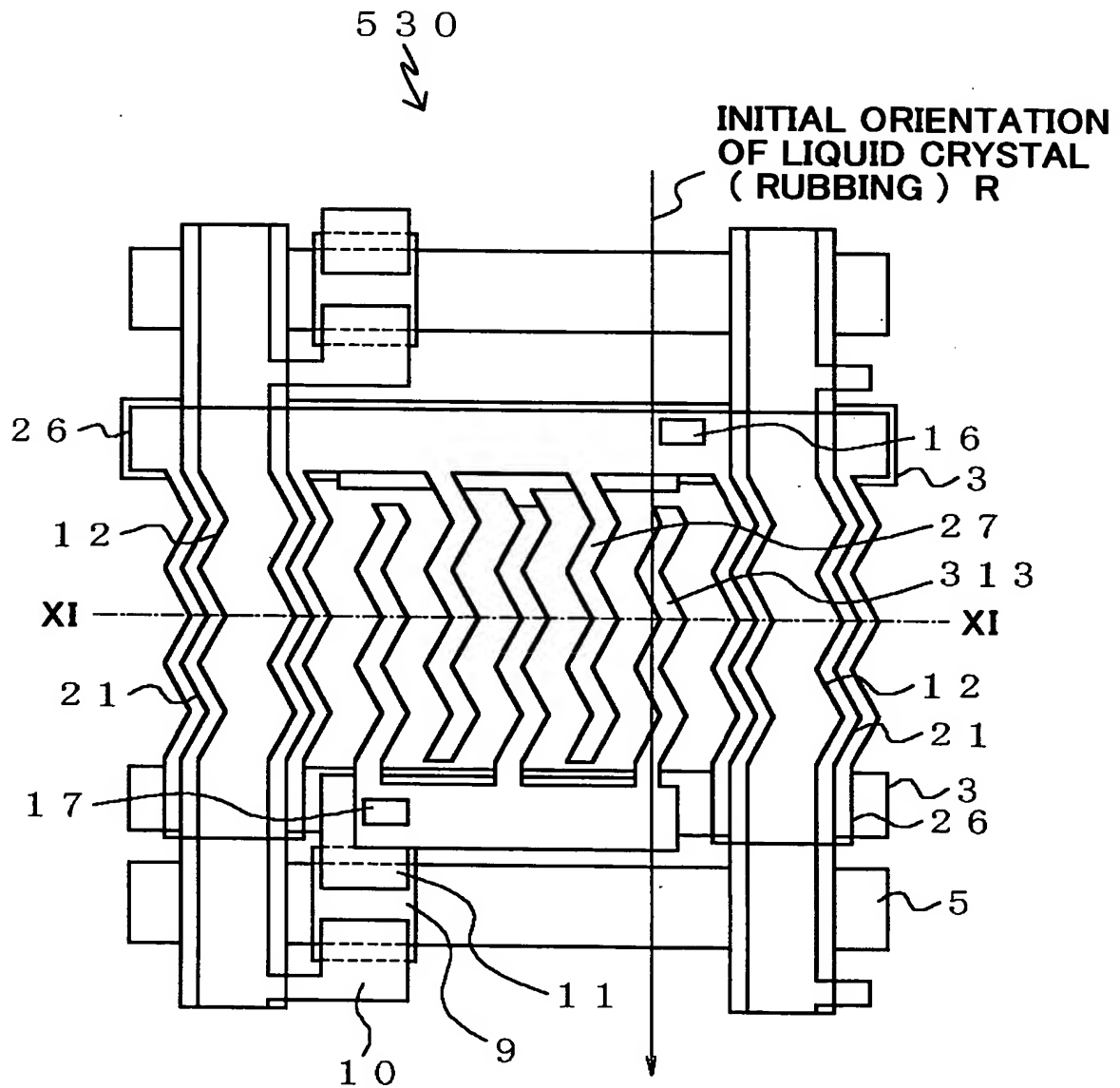
2 6

5

9/36

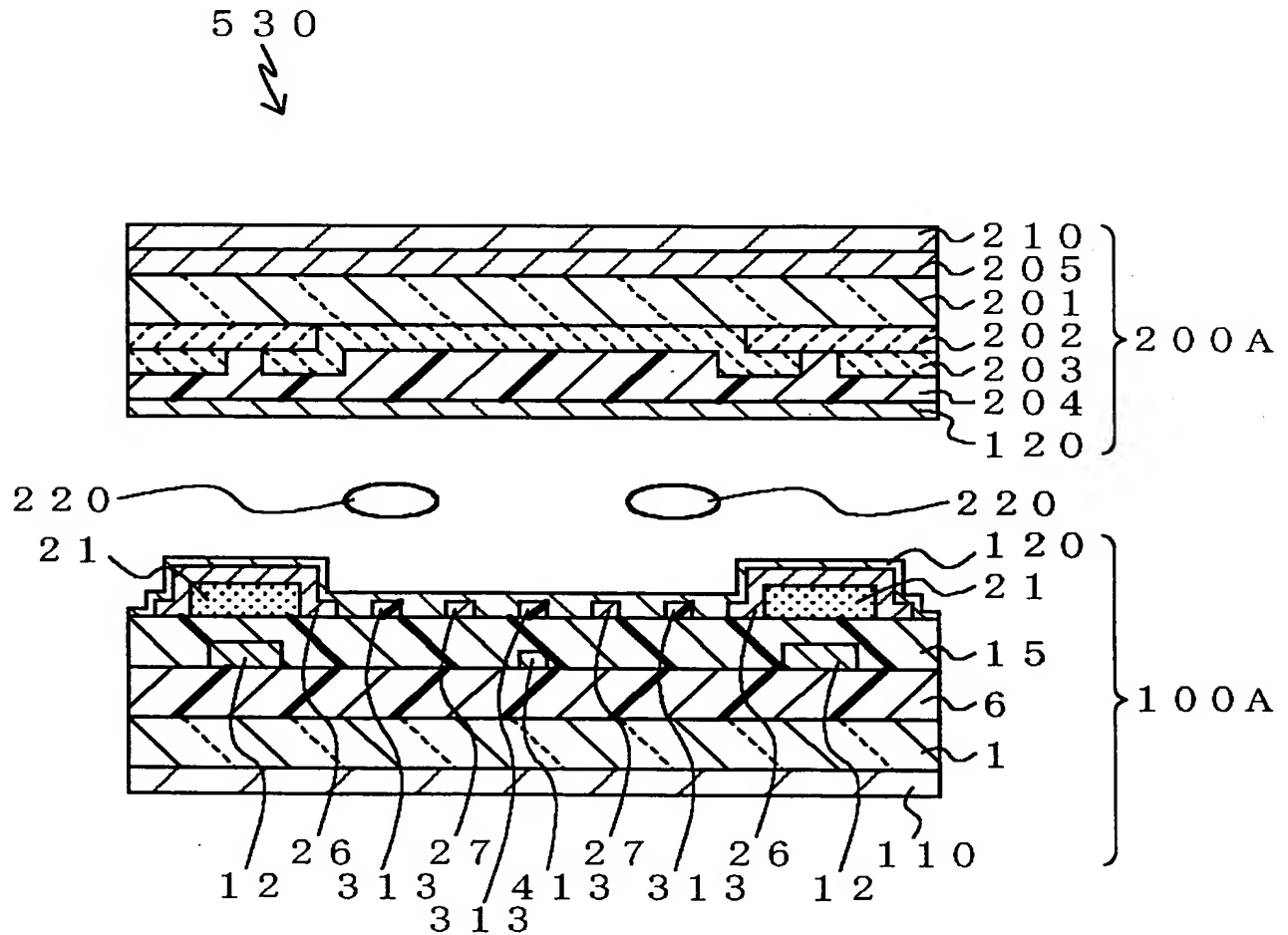
FIG.9





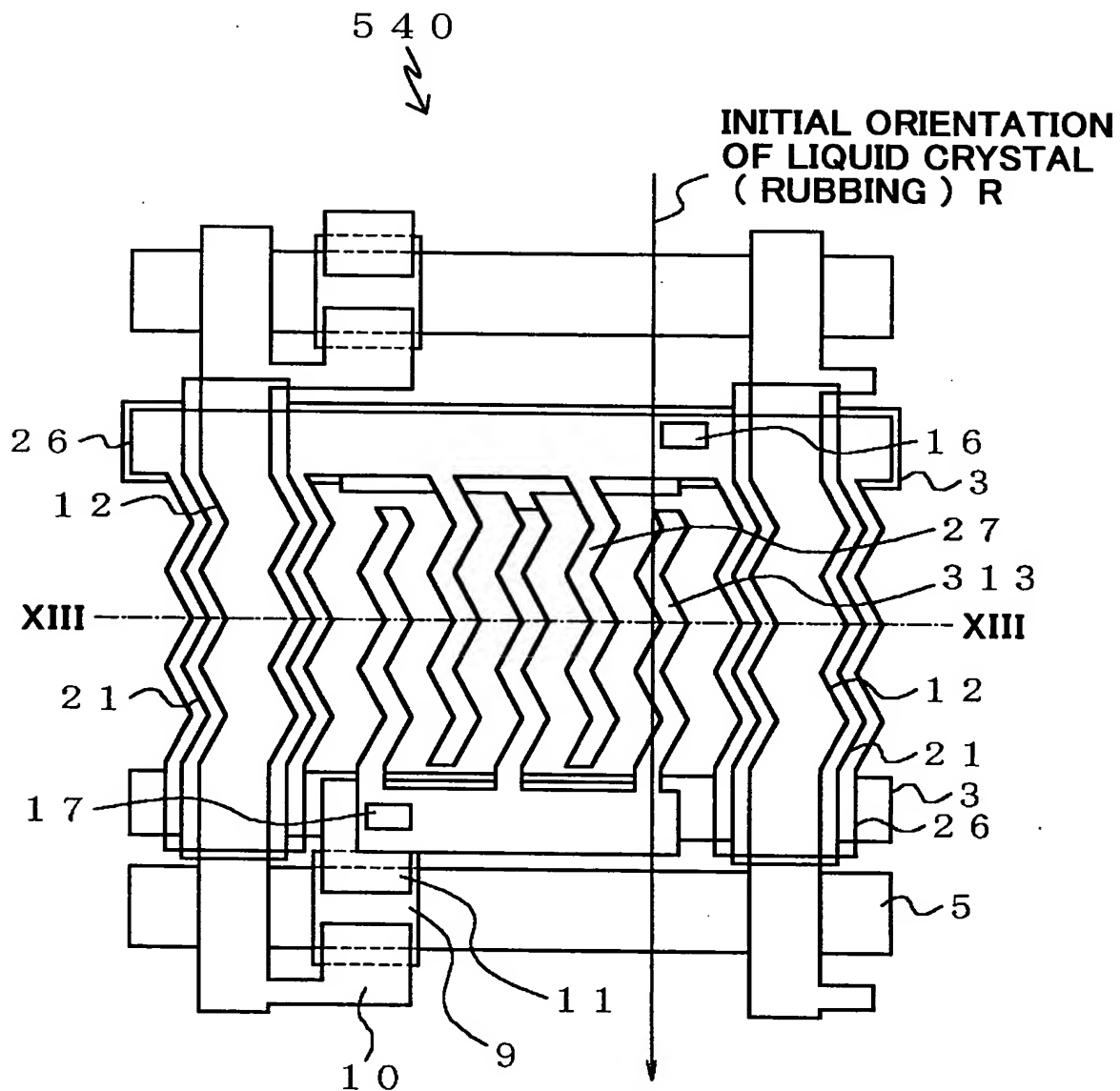
11/36

FIG.11



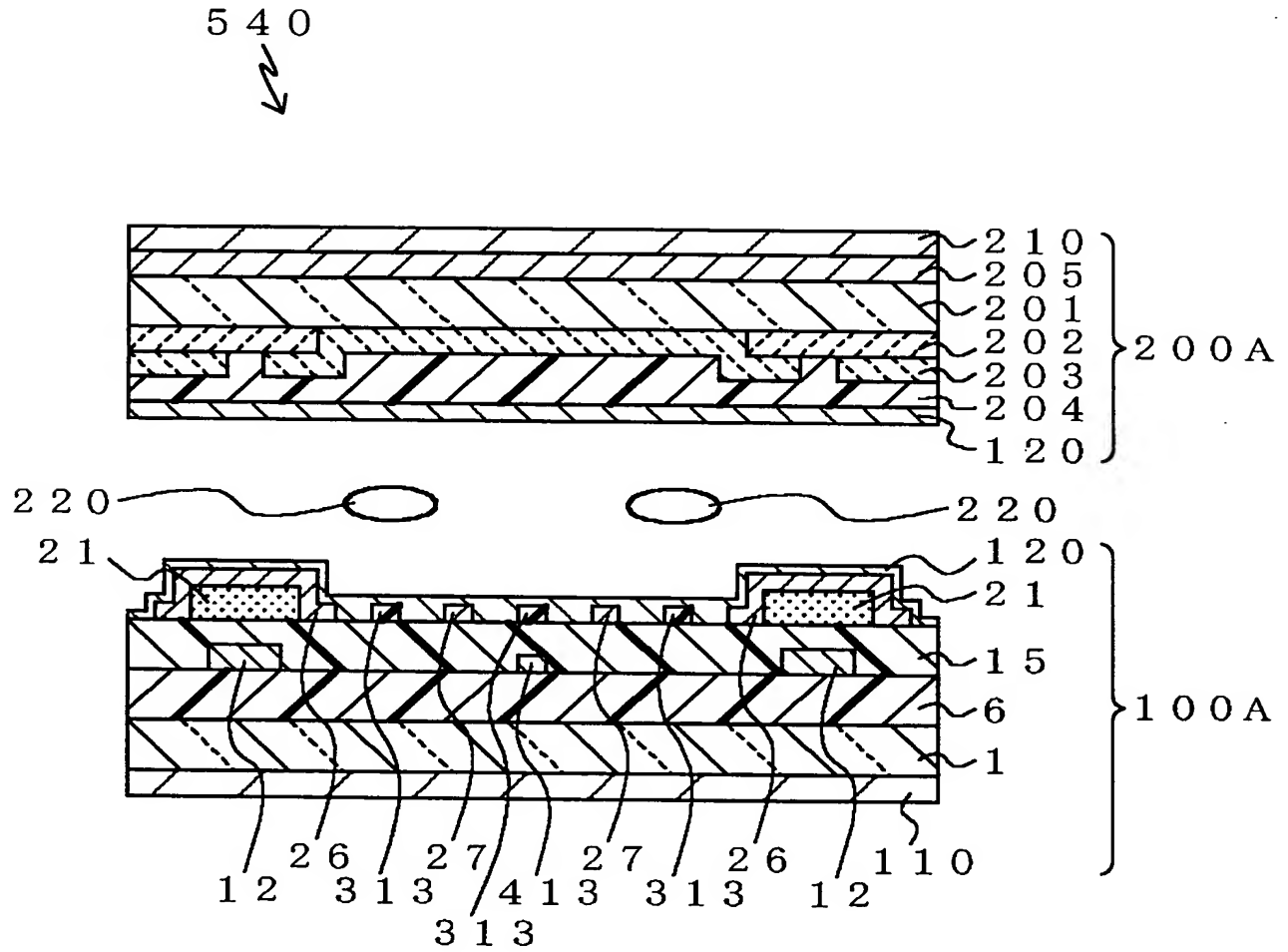
12/36

FIG.12



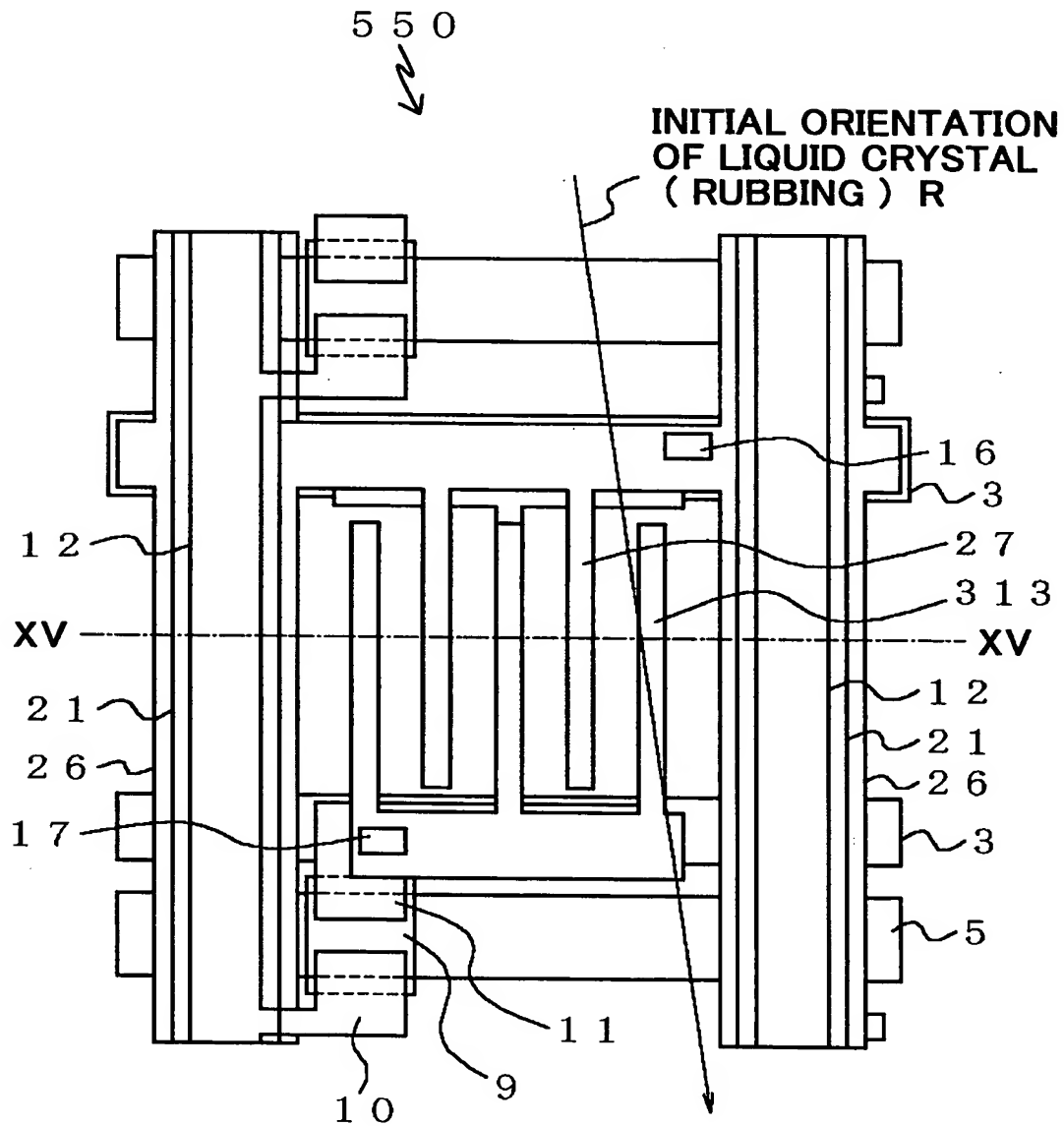
13/36

FIG.13



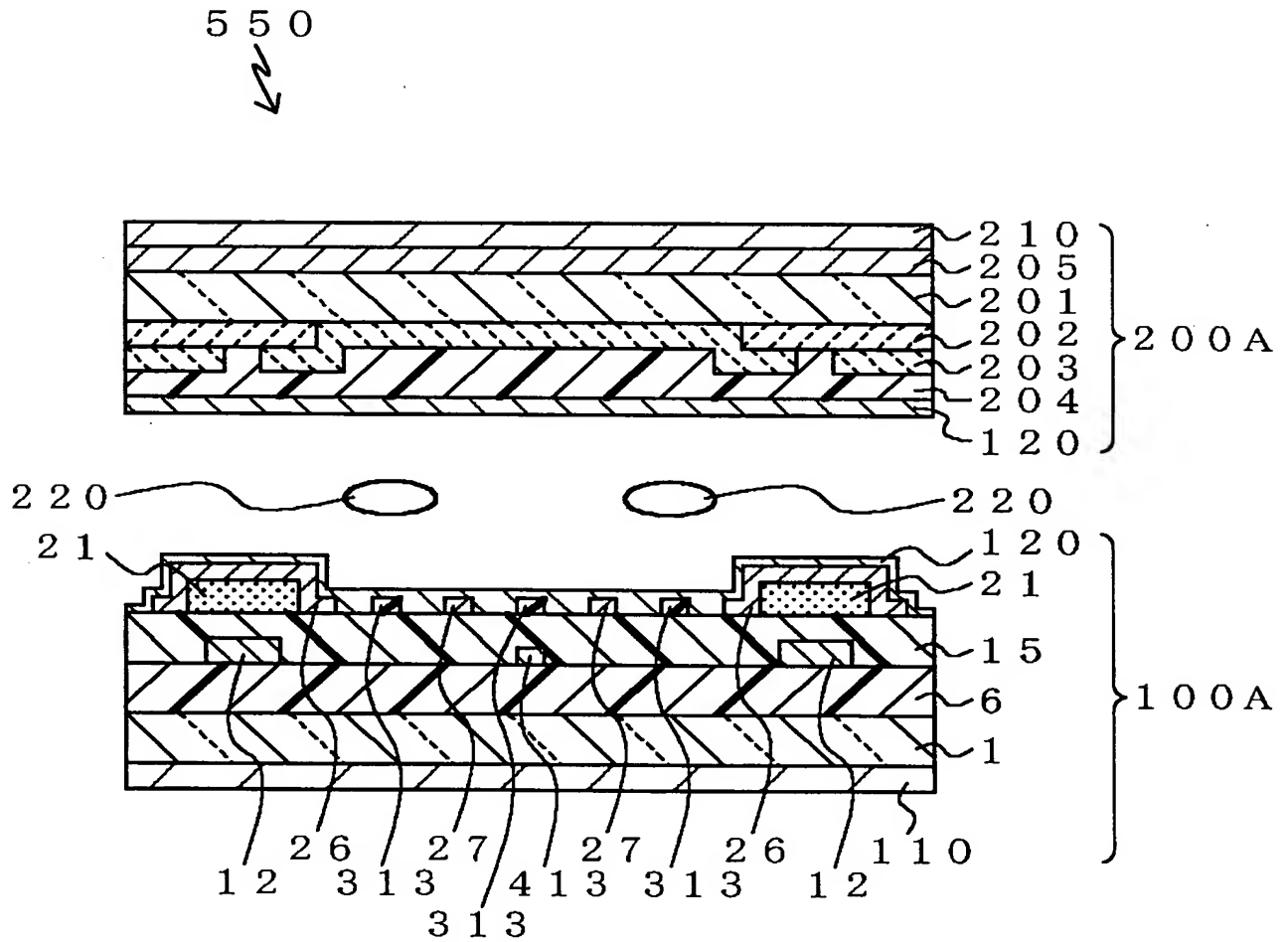
14/36

FIG.14

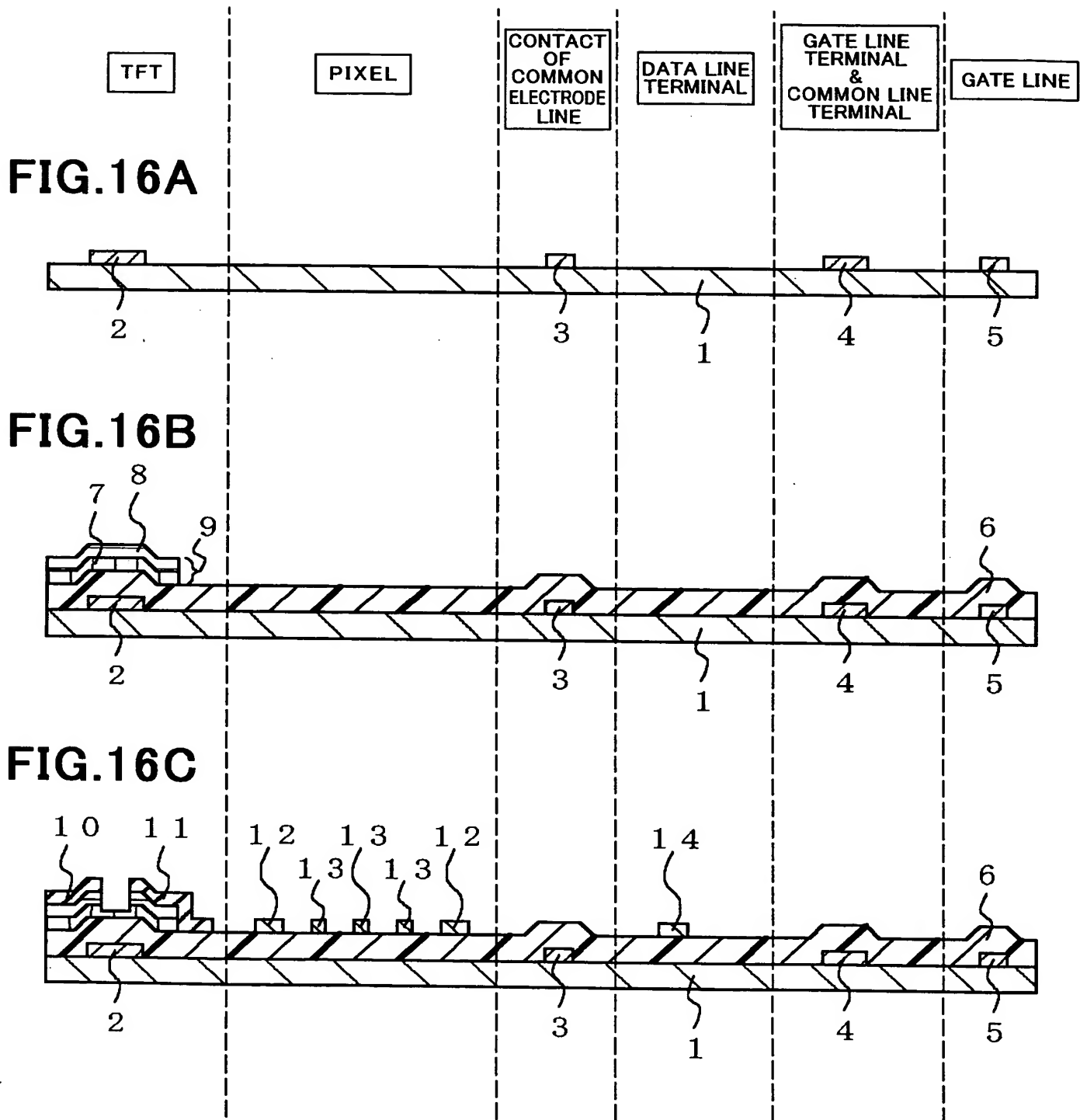


15/36

FIG.15



16/36



17/36

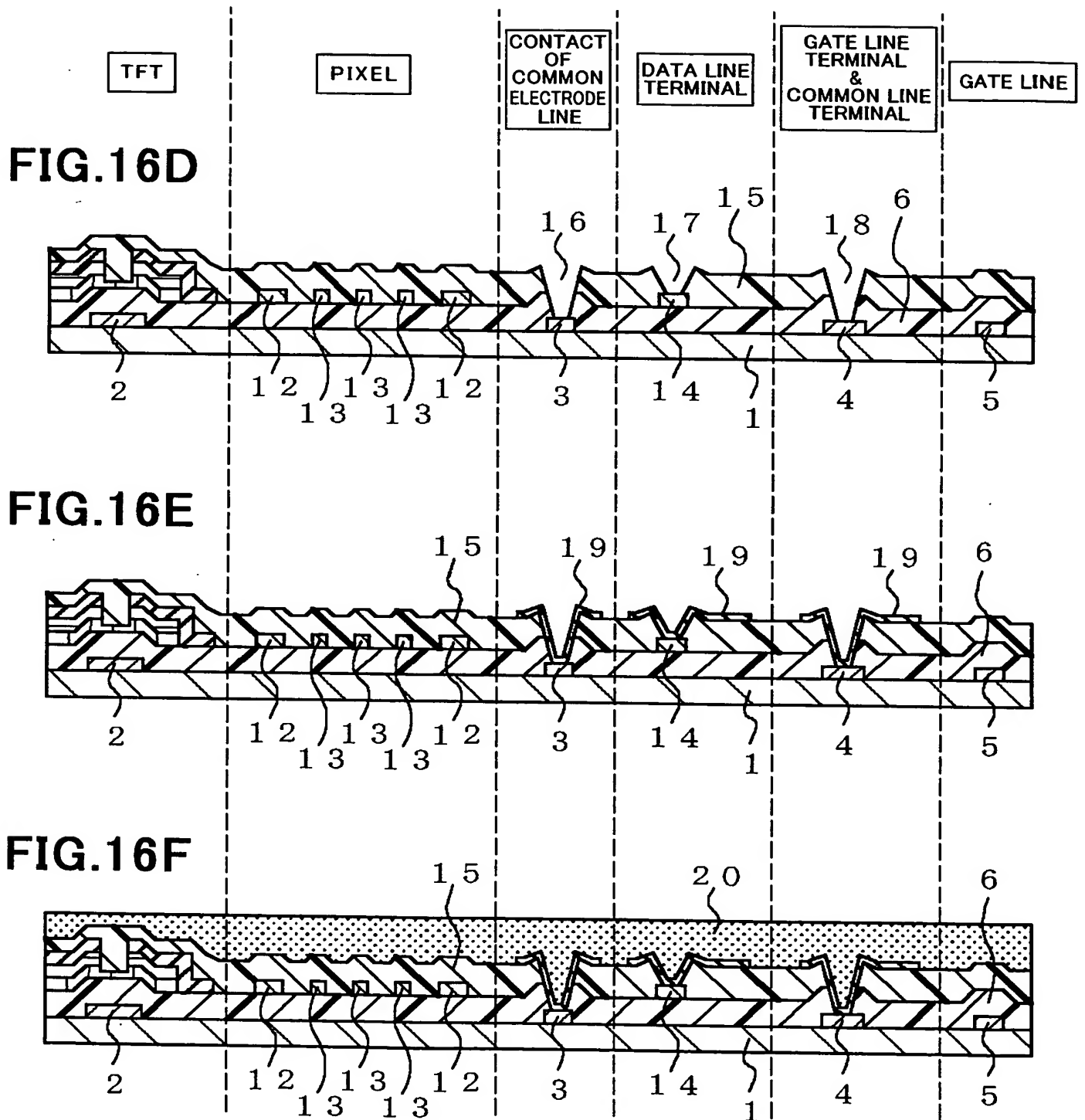


Figure 1G.16H is a cross-sectional view of a semiconductor device. It shows a series of gates (2) and contacts (1) on a substrate (2). The gates are formed by a sequence of layers: a base layer (2), a gate oxide layer (1), a gate stack (2), and a gate cap (1). The contacts are formed by a sequence of layers: a base layer (2), a contact oxide layer (1), a contact stack (2), and a contact cap (1). The device is shown in a cross-sectional view, with the gates and contacts arranged in a row.

19/36

FIG.17A

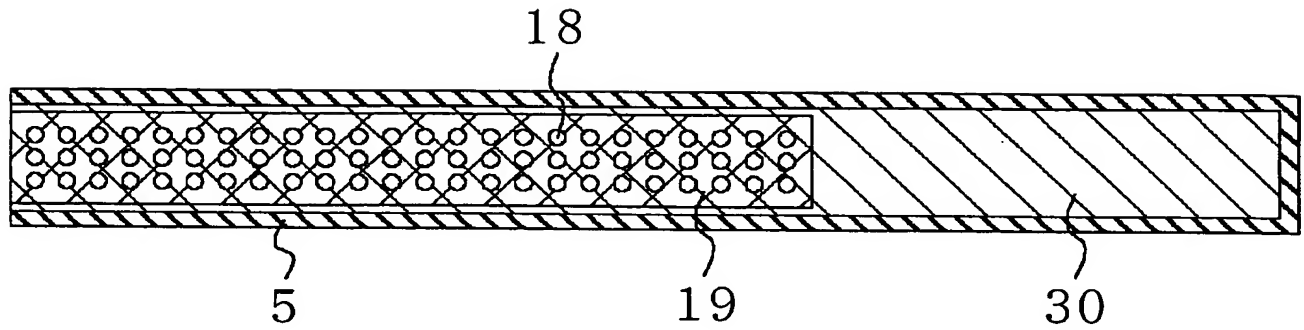
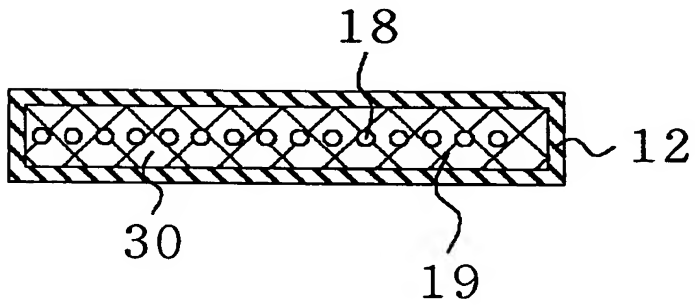
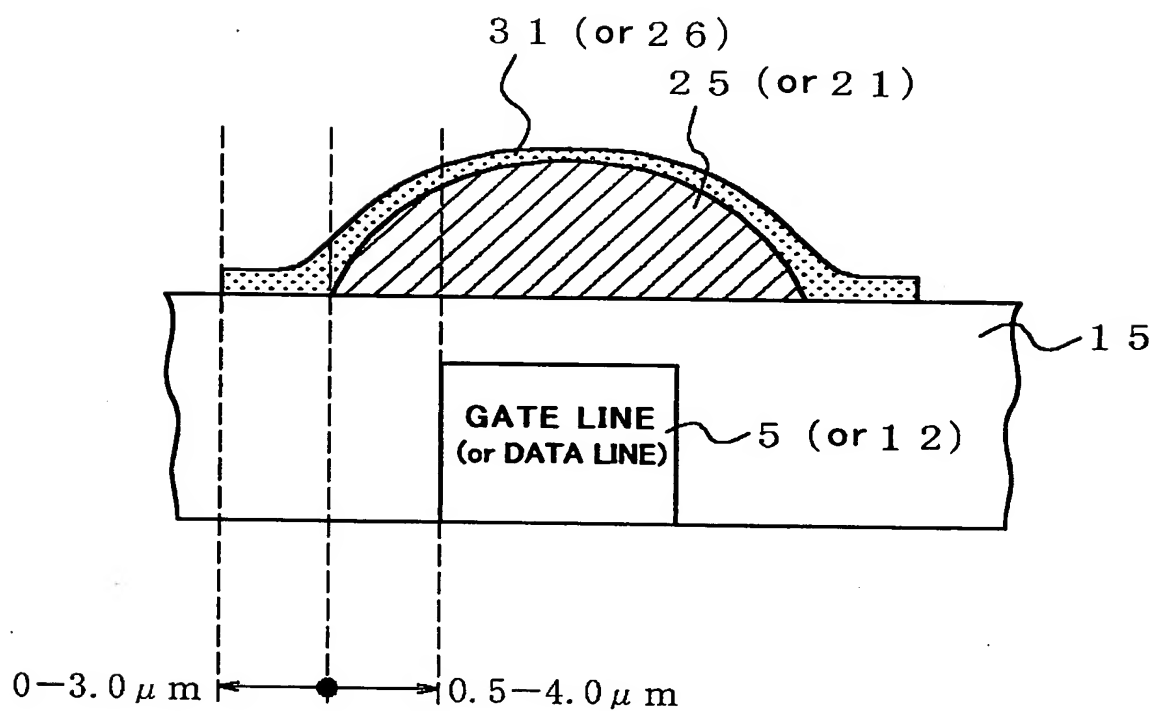


FIG.17B



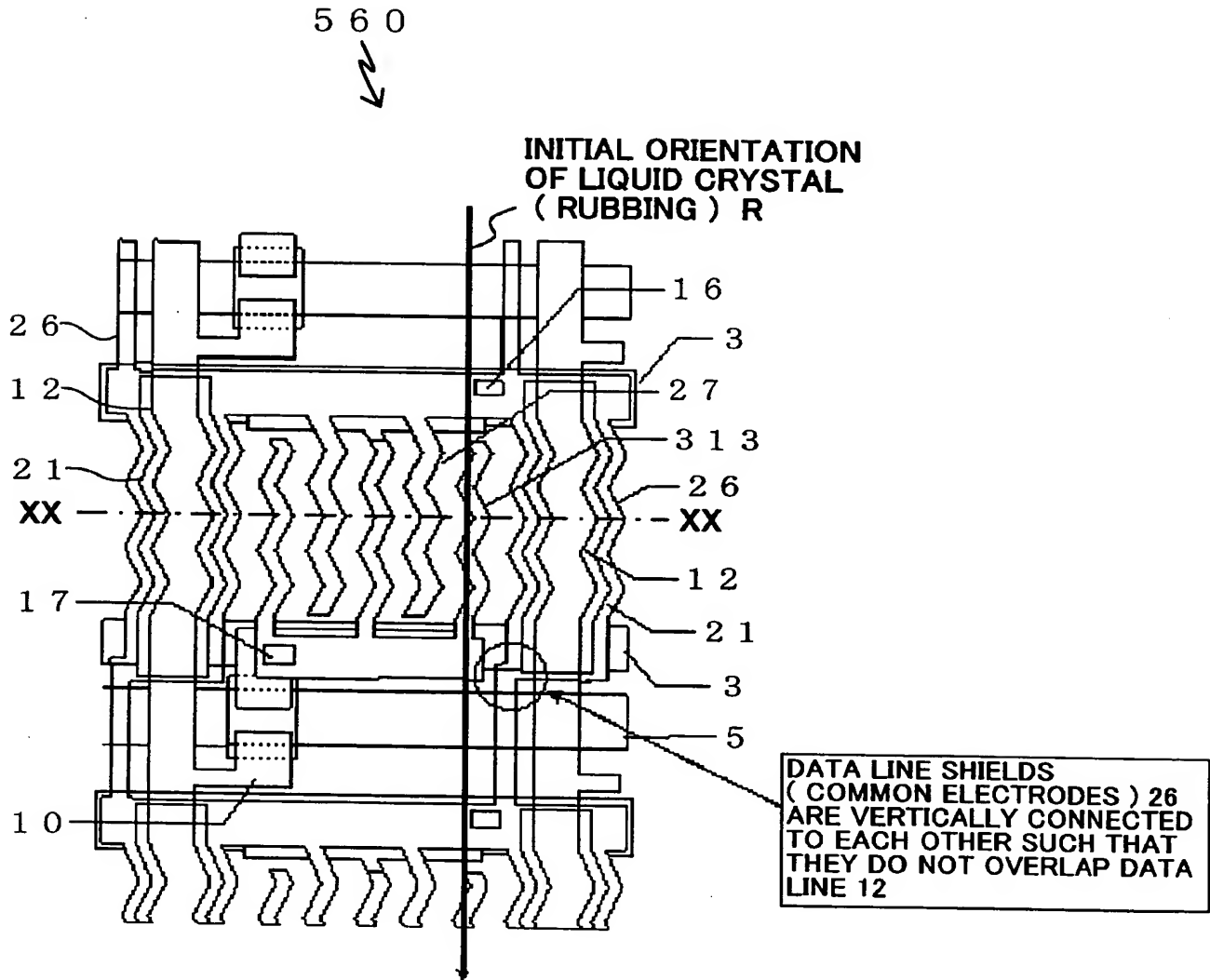
20/36

FIG.18



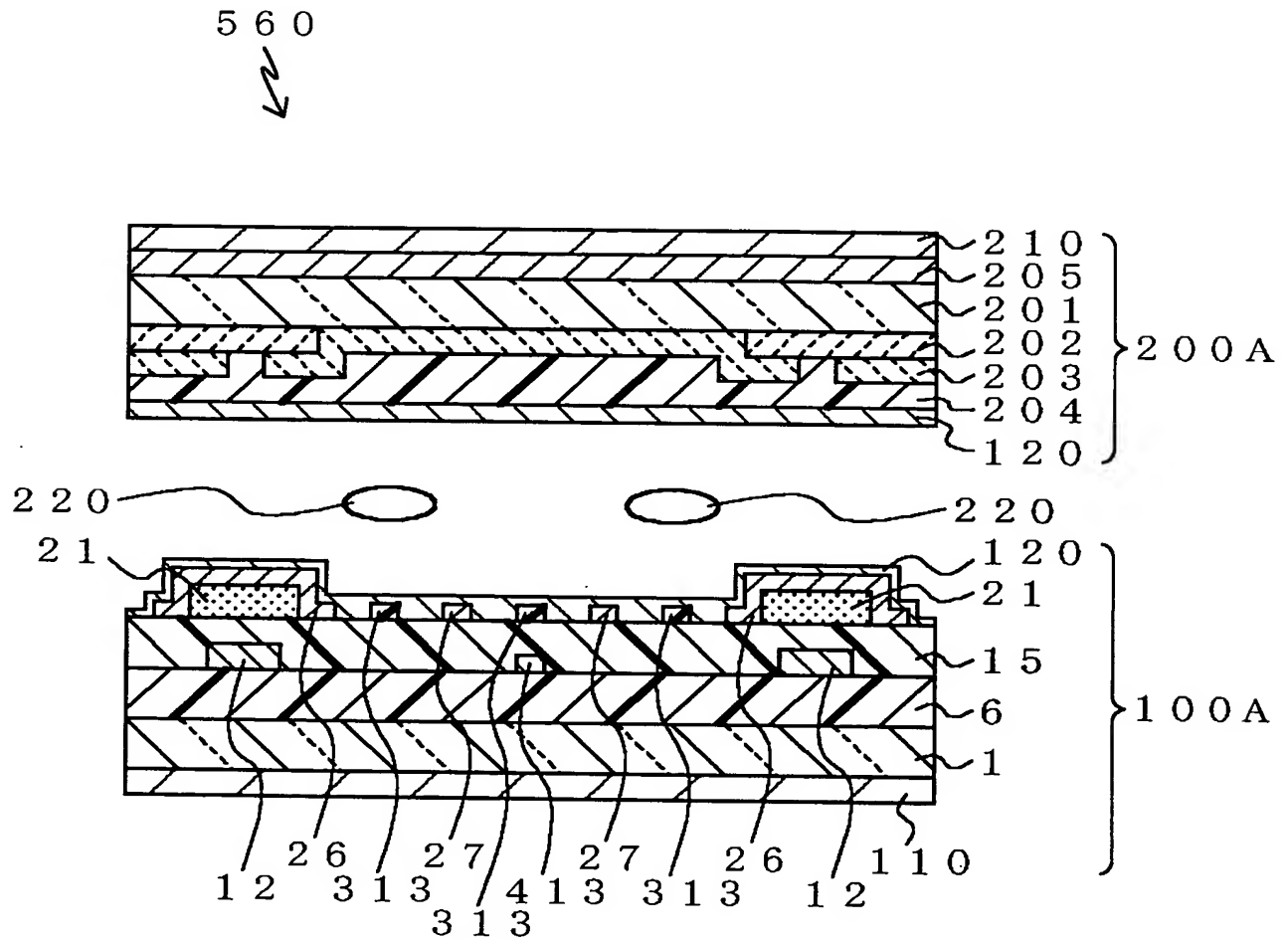
21/36

FIG.19



22/36

FIG.20



23/36

FIG.21A

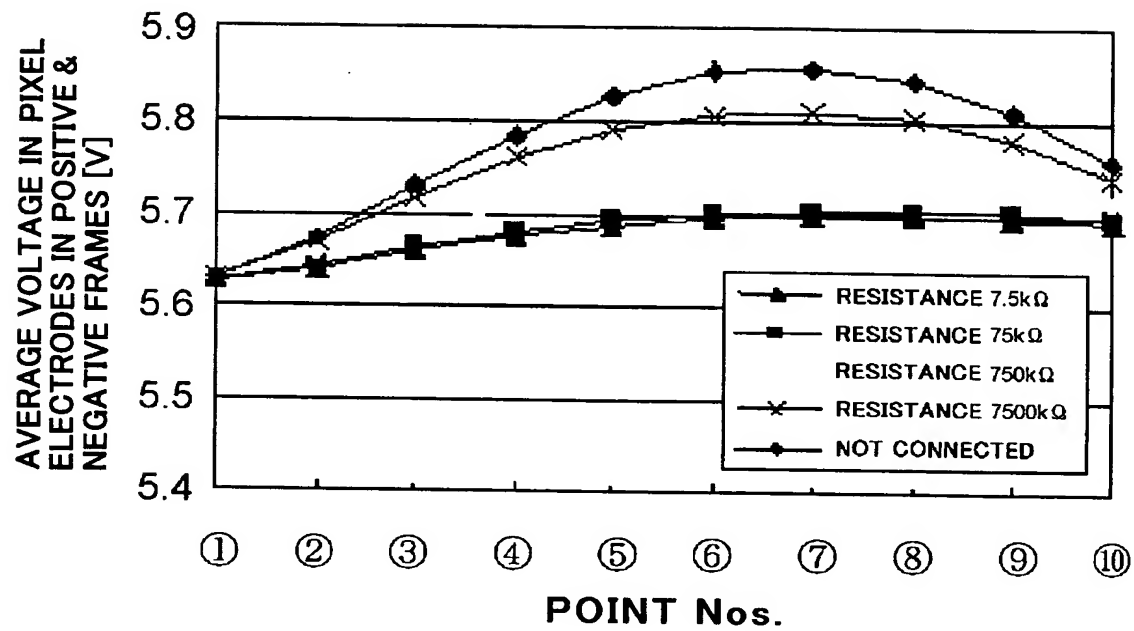
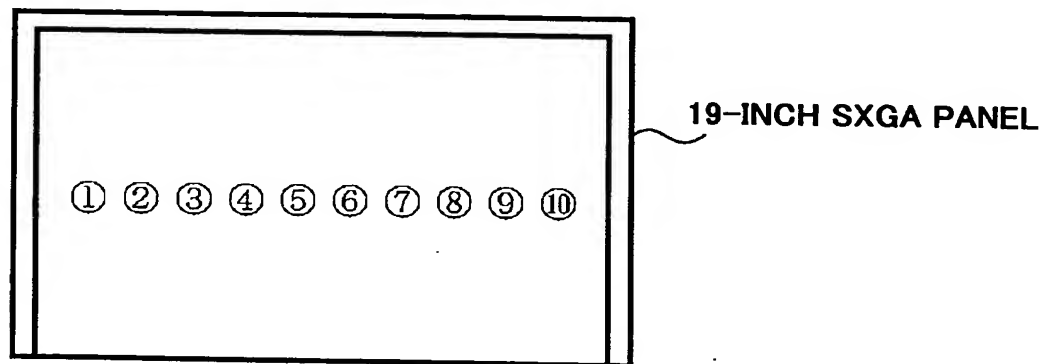
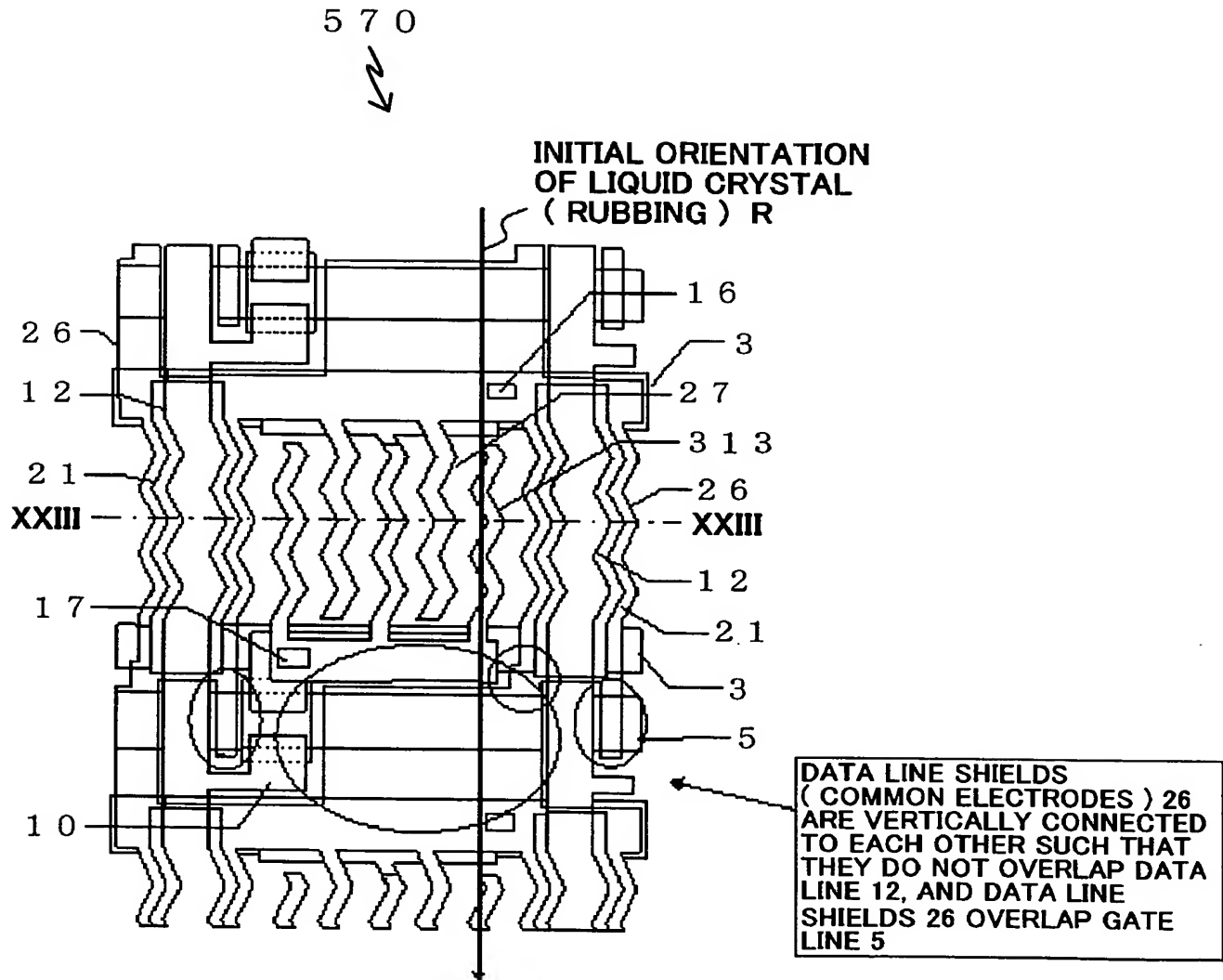


FIG.21B



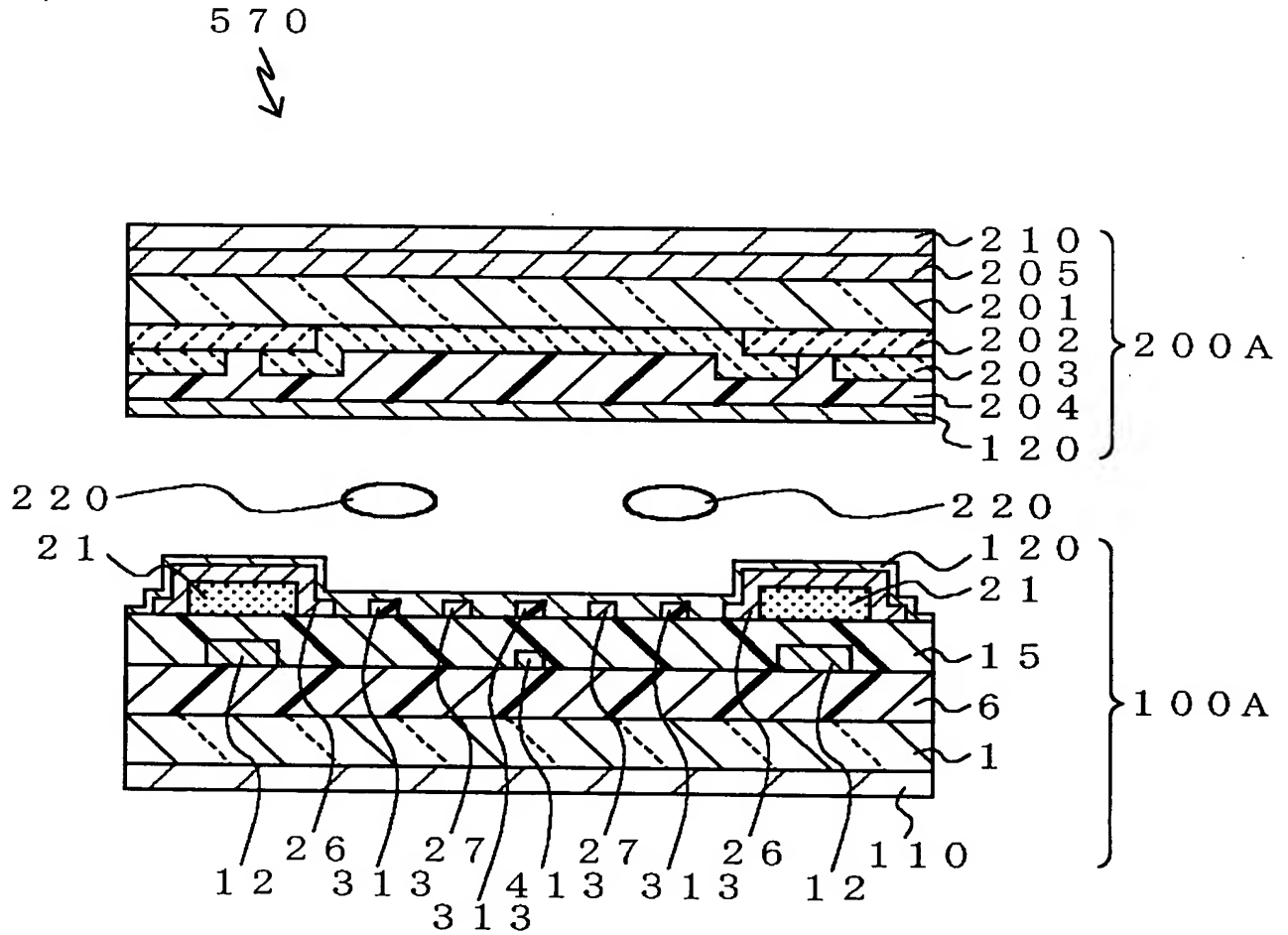
24/36

FIG.22



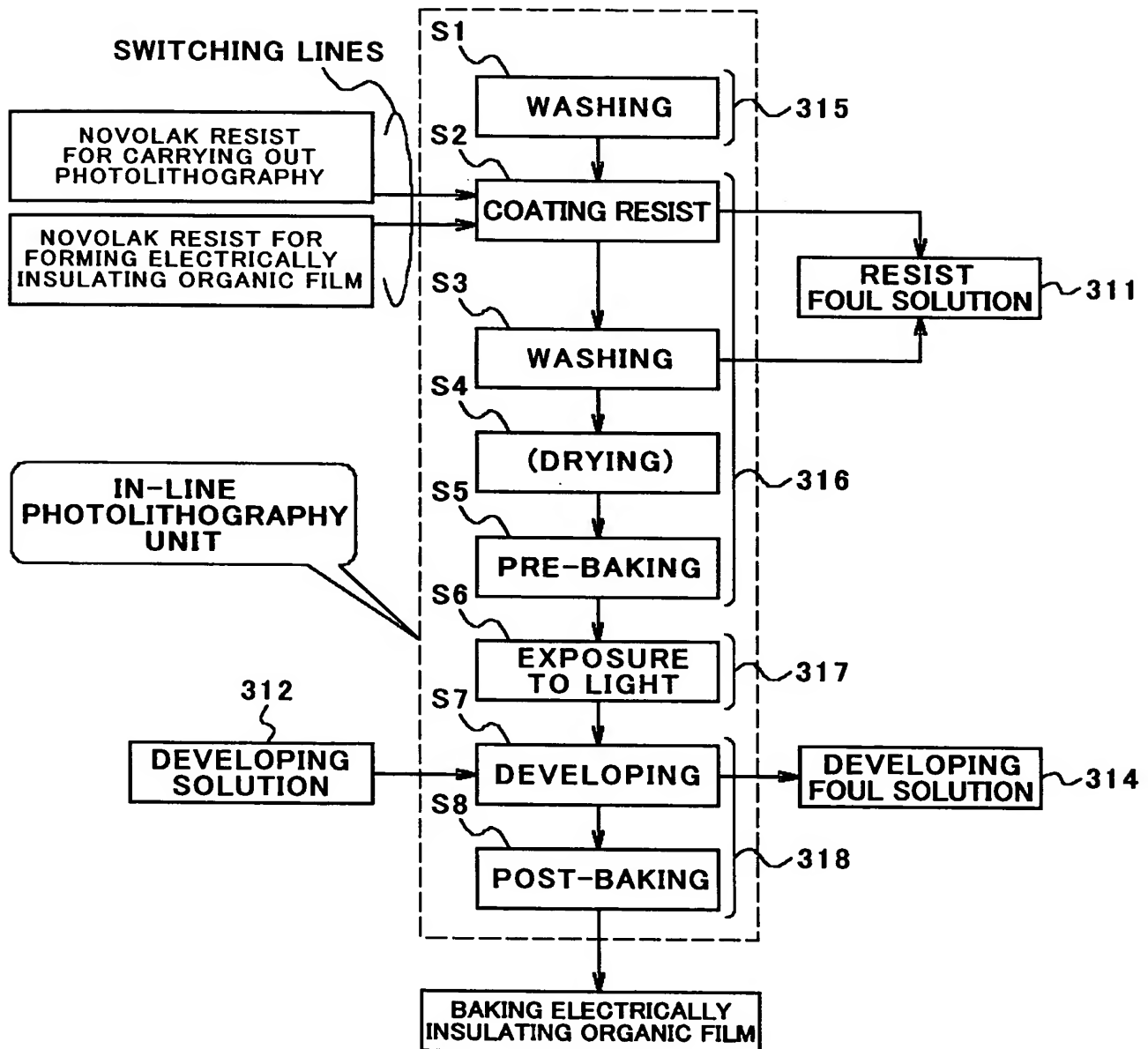
25/36

FIG.23



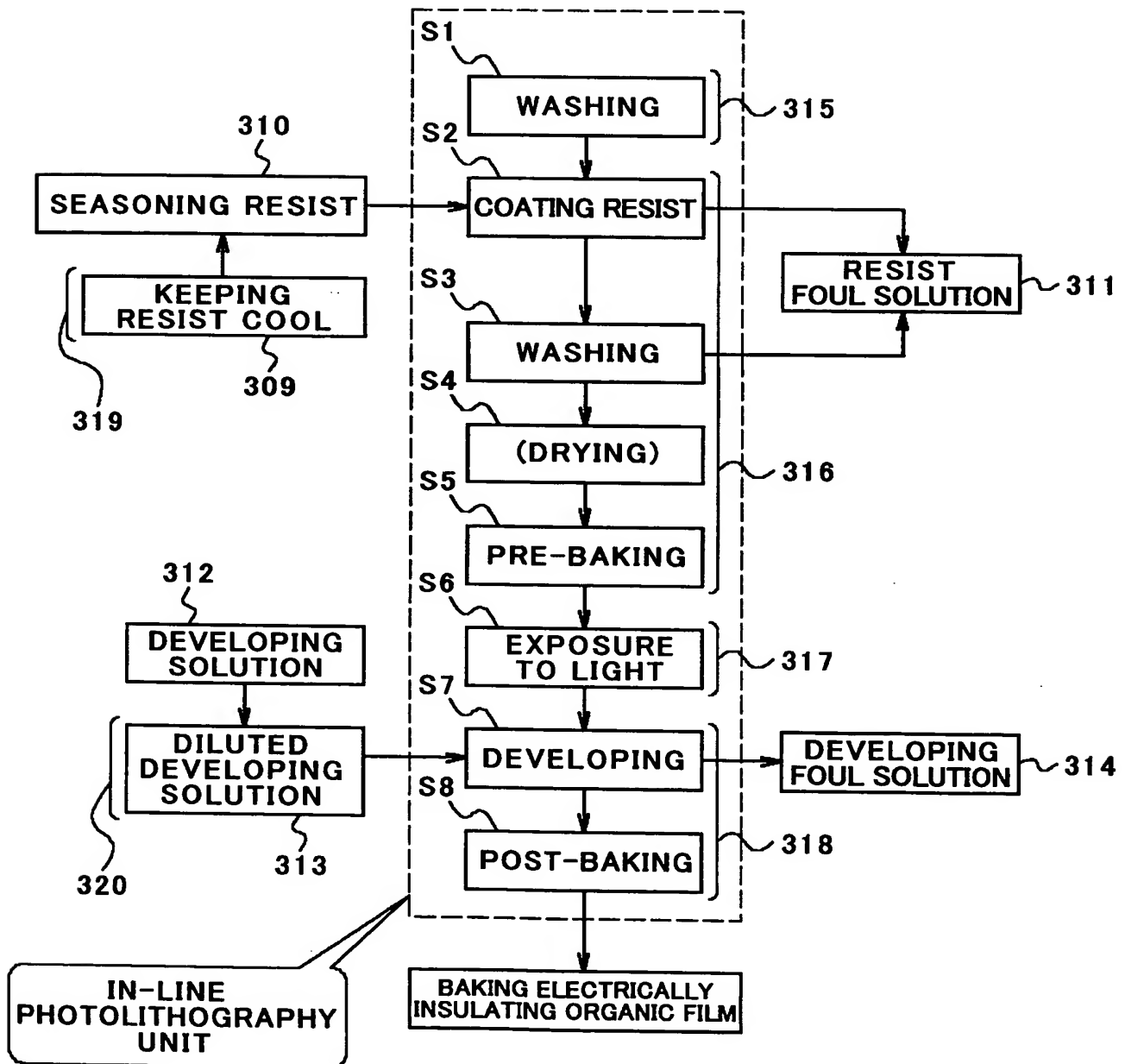
26/36

FIG.24



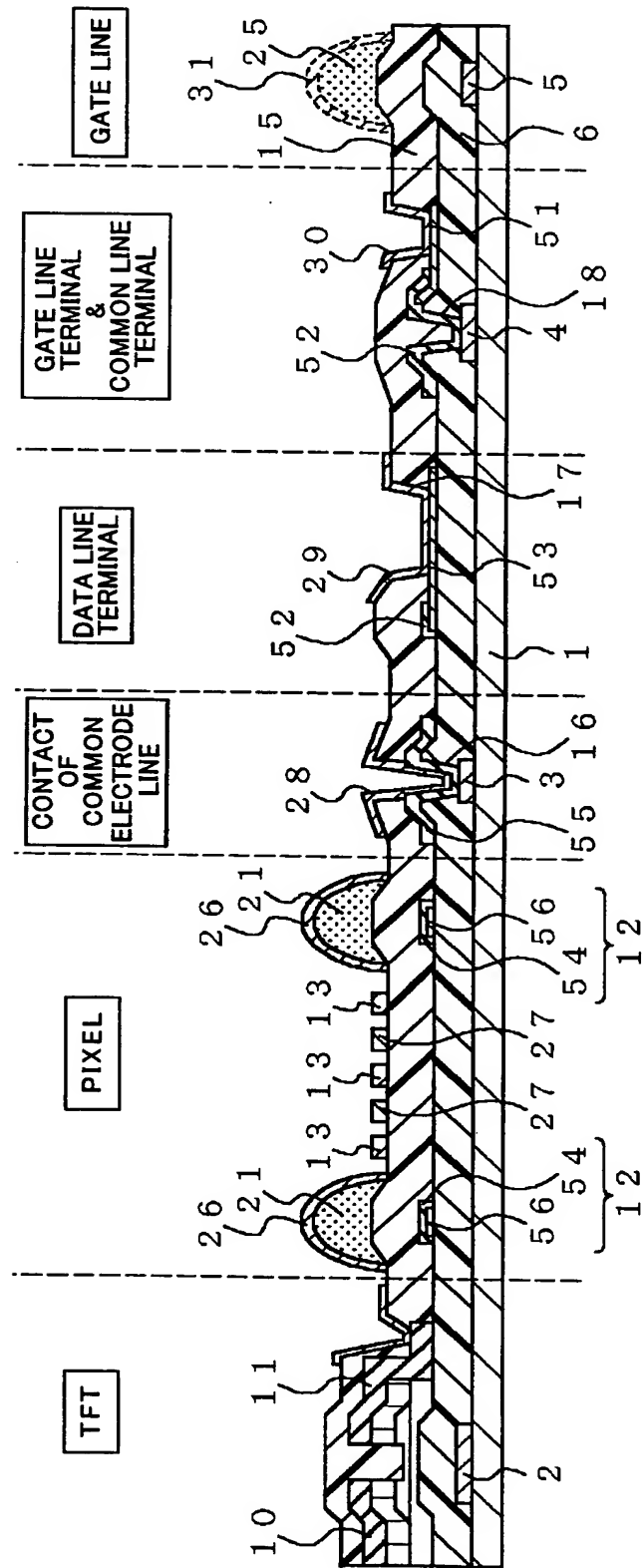
27/36

FIG.25



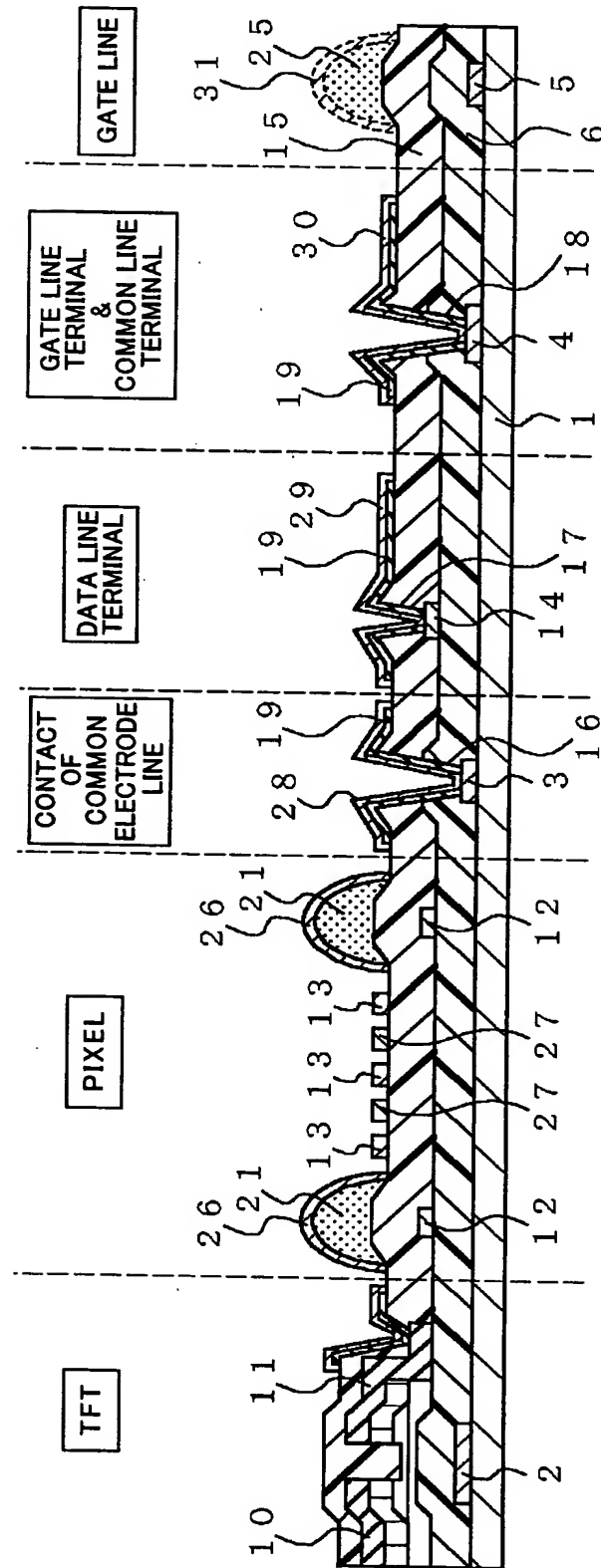
28/36

FIG. 26



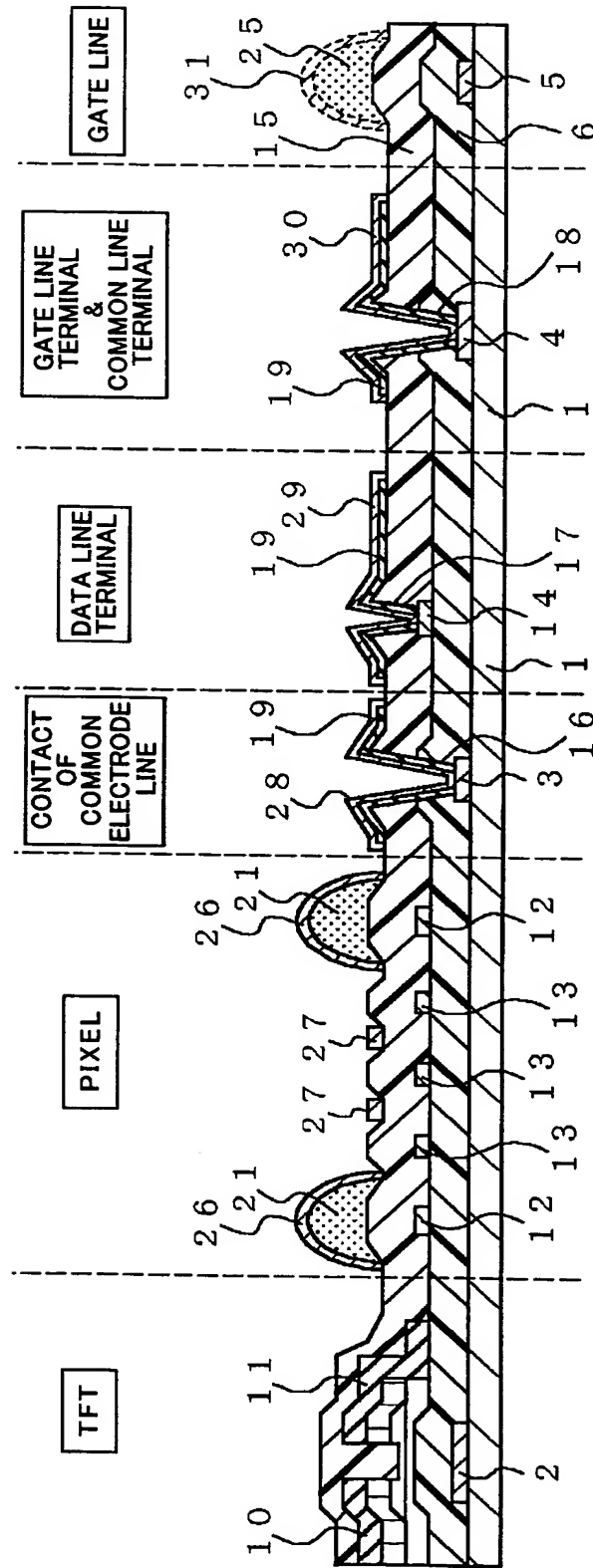
29/36

FIG.27



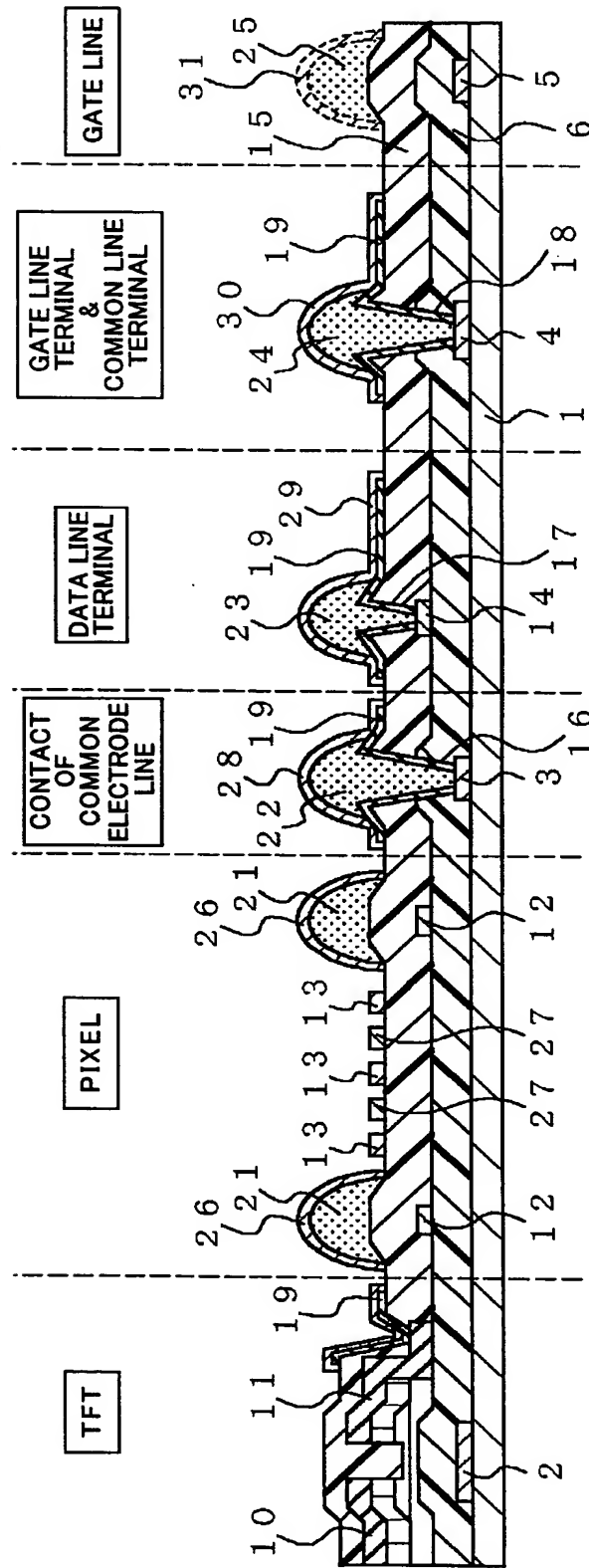
30/36

FIG.28



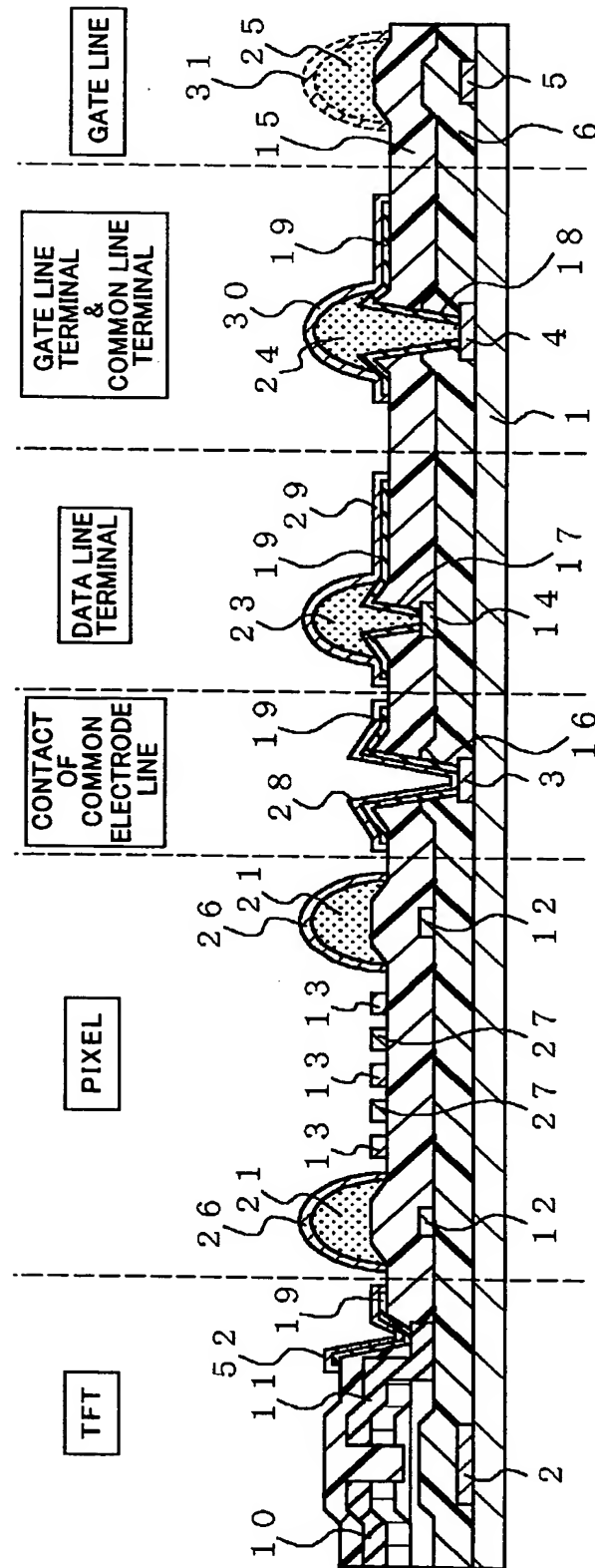
31/36

FIG.29



32/36

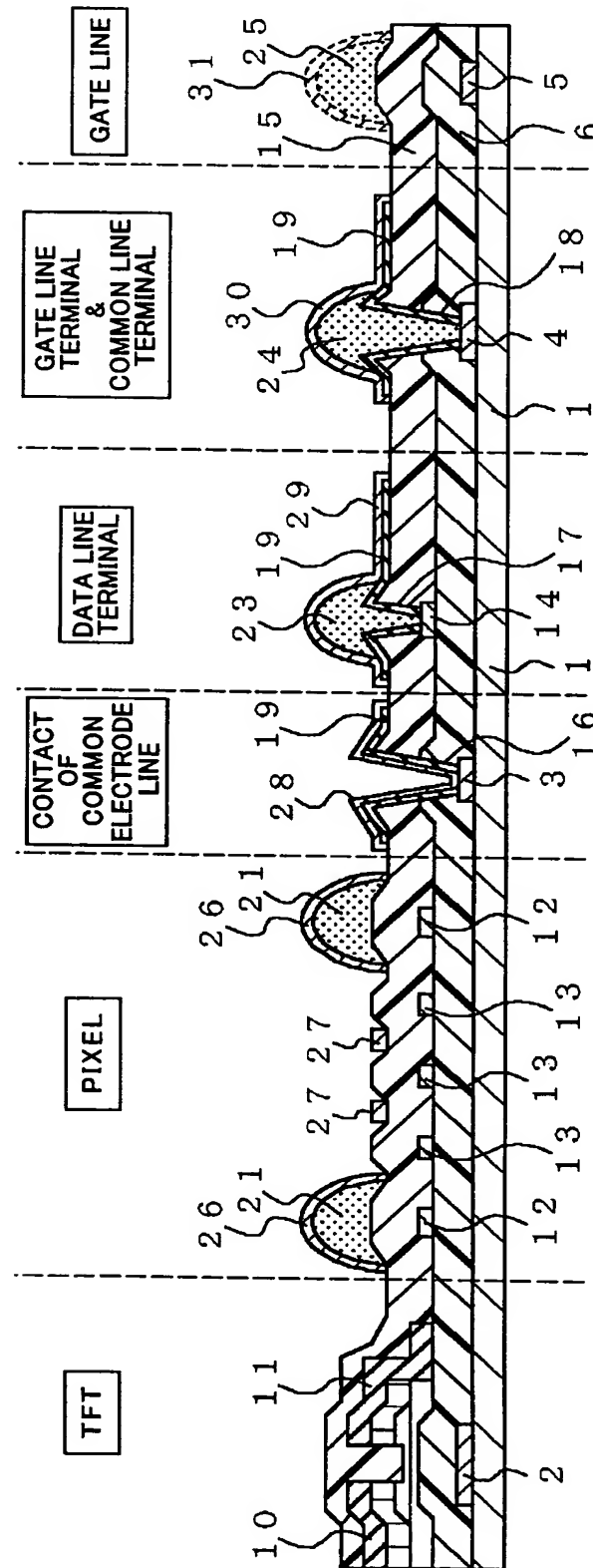
FIG.30



This cross-sectional view illustrates the structure of the TFT array substrate. It shows a pixel region on the left and a gate line terminal region on the right. The pixel region includes a pixel electrode (10) and a gate line (11). The gate line terminal region includes a gate line terminal (12) and a common line terminal (13). The diagram also shows a data line terminal (14) and a contact of common electrode line (15). Various layers and components are labeled with numbers: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31. The diagram is divided into sections by dashed lines, with labels: TFT, PIXEL, CONTACT OF COMMON ELECTRODE LINE, DATA LINE TERMINAL, GATE LINE TERMINAL & COMMON LINE TERMINAL, and GATE LINE.

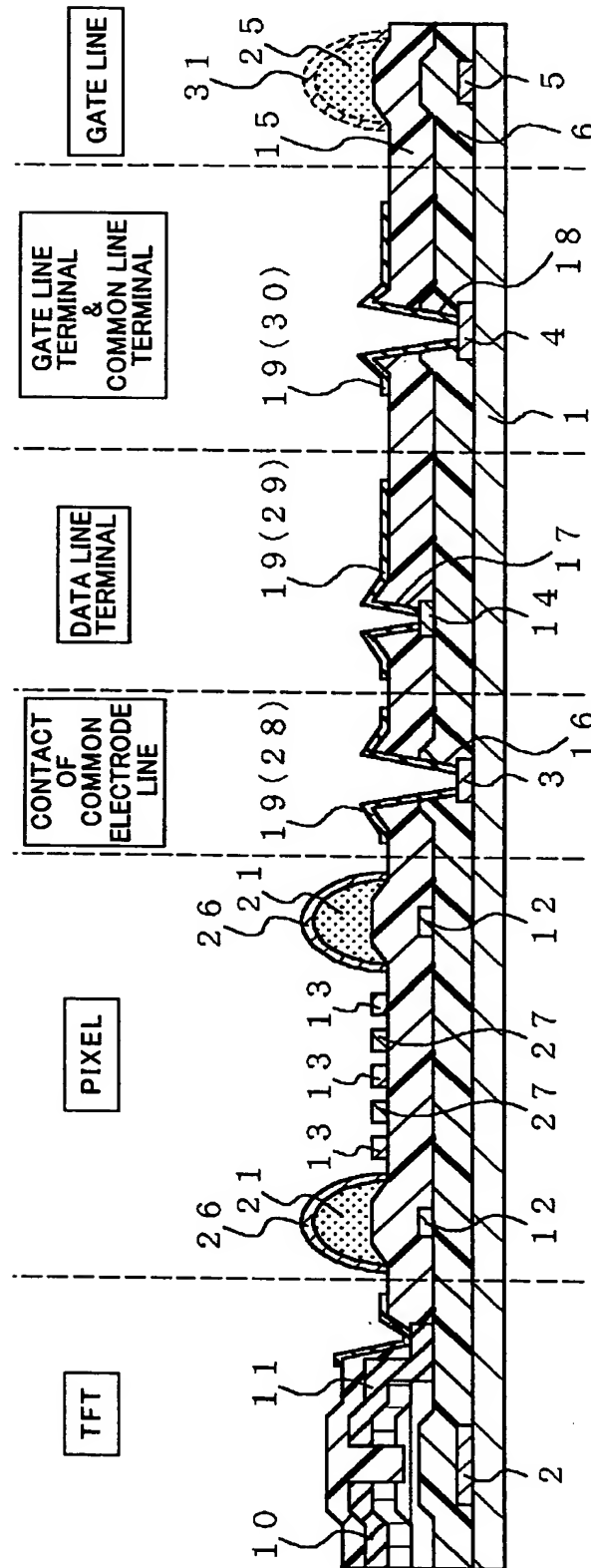
34/36

FIG.32



35/36

FIG.33



36/36

FIG.34

